

Modelling of a Switched Mode Power Supply using VHDL - AMS – A Hardware Descriptive Language

¹Meet Poladia, ²Dheeraj Pandey

^{1,2} PG Students

¹Department of Electronics and Telecommunication Engineering,
¹Sardar Patel Institute of Technology, Mumbai, India

Abstract - This paper provides an overview of the VHDL AMS hardware description language for analog and mixed-signal applications like the switched mode power supply which is designed by describing the major elements or components of the system with the help of this hardware descriptive language and illustrating it using Hamster which is a simulation software for VHDL and Verilog Descriptive Language.

Index Terms – SMPS, VHDL – AMS, Verilog AMS, analog simulations, mixed signal simulations.

I. INTRODUCTION

Hardware description languages (HDL's) are programming languages designed for describing the behavior of physical devices and processes, a task commonly called modelling. Models written in an HDL are used as input to a suitable simulator to analyze the behavior of the devices. HDL's have been used since the 1960's to model and simulate applications as diverse as digital and analog electronic systems, fluid concentrations in chemical processes, and parachute jumps.

Modern HDL's support the description of both behavior and structure. The structural mechanisms of an HDL allow a user to compose the model of a complete system from reusable model components stored in a library. Stored components are assembled into a design hierarchy that often closely resembles the decomposition of the system into subsystems and sub subsystems. The behavioral mechanisms of an HDL allow a user to express the operation of a subsystem at various levels of abstraction: very detailed, highly abstract, or anything in between. The designer can proceed using a top-down methodology, first performing conceptual studies using less detailed models, and then continually refining the design until each subsystem has been completed in sufficient detail for implementation. Top-down design and indefinite extensibility using stored components are the major advantages of an HDL based design methodology over traditional approaches.

In this contribution, we give an overview of VHDL-AMS, a new hardware description language for analog, digital, and mixed-signal applications. VHDL-AMS is an informal name for the combination of two IEEE standards: VHDL 1076-1993 and VHDL 1076.1-1999. In Section II introduces the elements of the language, focusing on the static semantics of the extensions introduced by IEEE Std. 1076.1-1999. Each language element is illustrated by examples. Finally, Section IV describes the modelling of the Switched Mode Power Supply with its simulation results.

II. OVERVIEW OF VHDL AMS MODELS

A VHDL-AMS model consists of an entity and one or more architectures. The entity specifies the interface of the model to the outside world. It includes the description of the ports of the model (the points that can be connected to other models) and the definition of its generic parameters. The architecture contains the implementation of the model. It may be coded using a structural style of description, a behavioral style, or a style combining structural, and behavioral elements. A structural description is a net list it is a hierarchical decomposition of the model into appropriately connected instances of other models. A behavioral description consists of concurrent statements to describe event-driven behavior and simultaneous statements to describe continuous behavior. Concurrent statements include the concurrent signal assignment for data flow modeling and the process statement for more general event-driven modeling.

When a VHDL-AMS model is instantiated in a structural description, the designer can specify which of several architectures to use for each instance. Alternatively, the decision can be postponed until immediately prior to the simulation. This allows for an easy and flexible reconfiguration of the model. For example, in top-down design, one architecture can describe a subsystem behaviorally with little detail, while another can add parasitic and a third can decompose the subsystem into lower level components.

Quantities

The unknowns in the collection of DAE's implied by the text of a model are analytic functions of time; that is, they are piecewise continuous with a finite number of discontinuities. The analog solver solves for the values of all unknowns over time by first converting, at specific values of time, the differential part of the DAE's to algebraic equations using appropriate discretization methods, and then solving the algebraic equations simultaneously.

VHDL-AMS introduces a new class of objects, the quantity, to represent the unknowns in the DAE's. Quantities can be scalar or composite (arrays and records), but must have scalar sub elements of a floating-point type. A quantity object can appear anywhere a value of the type is allowed, in particular in an expression. In the remainder of this section, we describe the

characteristics of scalar quantities. The characteristics of a composite quantity are simply the aggregation of the characteristics of its scalar sub elements. The behavior of each scalar sub element is independent of the others.

Quantities can be declared anywhere a signal can be declared except in a VHDL package. The following statement declares three quantities q1, q2, and q3 of type REAL:

quantity q1,q2,q3: REAL

where bold text indicates reserved words and upper-case text indicates predefined concepts.

Simultaneous Statement

Simultaneous statements are a new class of statements in VHDL-AMS for notating differential and algebraic equations. Simultaneous statements contain ordinary VHDL expressions that can be evaluated in the ordinary way. Simultaneous statements can appear anywhere a concurrent signal assignment is allowed. The basic form is the simple simultaneous statement, which has the following syntax:

[label :] expression = expression

where the square brackets indicate that this part of the statement is optional.

Several additional forms of the simultaneous statement have been defined. The simultaneous case statement and simultaneous if statement are analogous to their sequential counterparts and allow the description of piecewise defined behavior. Each contains an arbitrary list of simultaneous statements in its statement parts, including nested simultaneous case and if statements. The analog solver considers only the simultaneous statements selected by the case expressions and chosen by the conditional expressions. The simultaneous procedural statement is merely a way to rewrite the function body *f* in the simultaneous statement *f(q,x) = q* "in line," where *q* is a collection of quantities and *x* is an arbitrary collection of other objects.

Modelling of a Resistor using VHDL AMS

In VHDL AMS, the model comprises of two sections that is the entity and the architecture. In this section we will see the modelling of a passive resistor using the VHDL AMS. Fig. 1 shows basic symbol of a resistor where p1 and p2 are two end points and as we all know that the resistor works on the principal of ohms law i.e $V = I \cdot R$. Fig 2 and 3 show the entity and architecture declarations of a resistor. In the same manner all the other components can be modelled using both VHDL AMS or Verilog AMS HDL's.

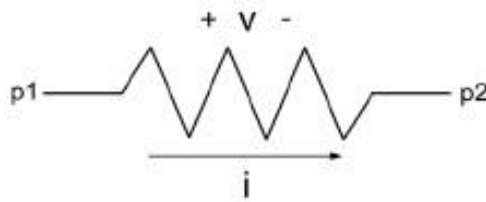


Fig. 1 Symbol of a Resistor

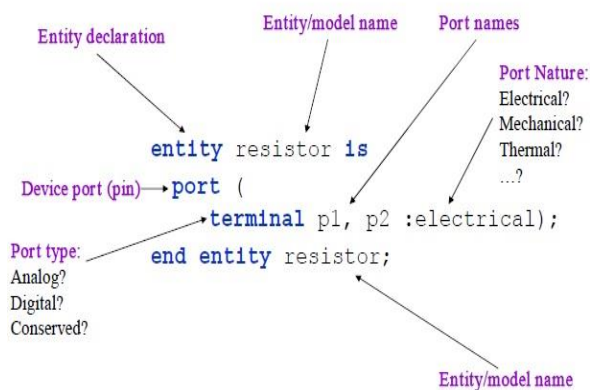


Fig. 2 Entity Declaration

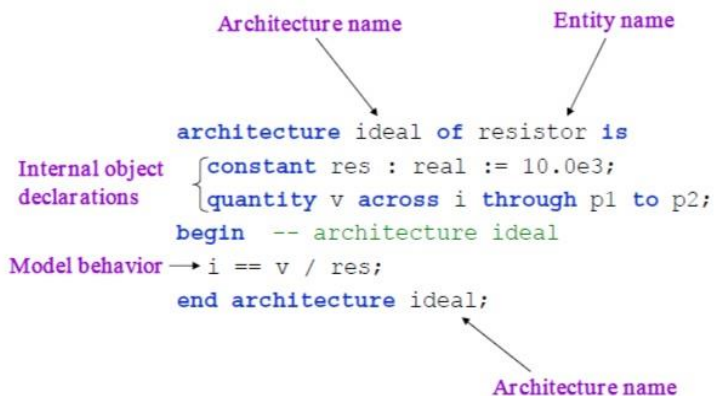


Fig 3 Architecture Declaration

III. MODELLING OF SMPS

A **switched-mode power supply** is an electronic power supply that incorporates a switching regulator to convert electrical power efficiently. Like other power supplies, an SMPS transfers power from a source, like mains power, to a load, such as a personal computer, while converting voltage and current characteristics. Unlike a linear power supply, the pass transistor of a switching-mode supply continually switches between low-dissipation, full-on and full-off states, and spends very little time in the high dissipation transitions, which minimizes wasted energy. Ideally, a switched-mode power supply dissipates no power. Voltage regulation is achieved by varying the ratio of on-to-off time.

The model of SMPS in Fig. 4 beats the SPICE model due to its complexity and a very large number of time-points required by its disparate time scales. The behavioral model of the switch controller in the VHDL-AMS implementation simplifiers vastly both the analog and digital (i.e. algorithmic) part of the circuit and hence enables fast and accurate simulation of switch-mode power

regulation.

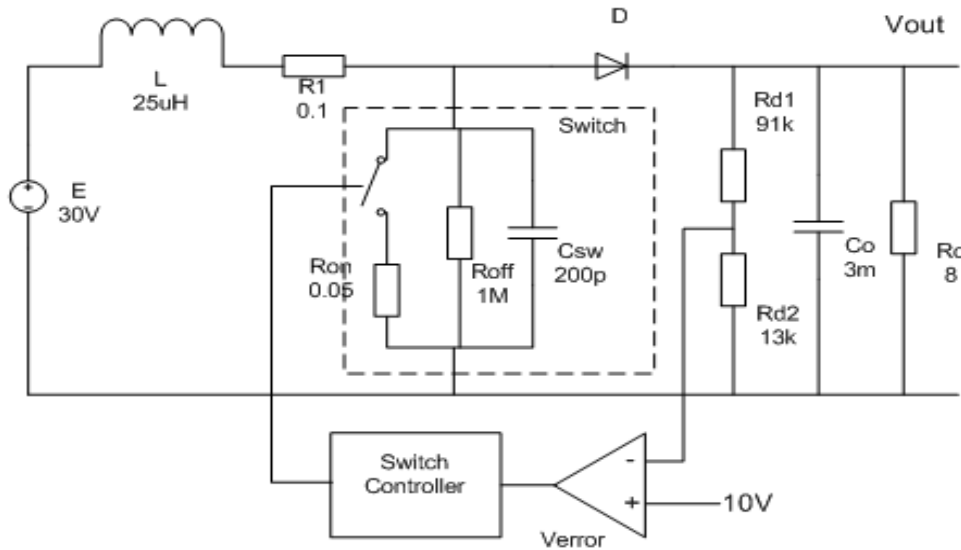


Fig. 4 Simulation Model of a SMPS.

<p>Modelling of an Inductor</p> <pre> library IEEE; use IEEE.electrical_systems.all; entity inductor is generic (ind : inductance); -- Nominal inductance port (terminal p1, p2 : electrical); end entity inductor; architecture ideal of inductor is -- Declare Branch Quantities quantity v across i through p1 to p2; begin if domain=quiescent_domain use --set initial condition i==0.0; else v == ind * i'dot; -- Fundamental equation end use; end architecture ideal; </pre>	<p>Modelling of a Capacitor</p> <pre> library IEEE; use IEEE.electrical_systems.all; entity capacitor is generic (cap: capacitance); -- Capacitance [F] port (terminal p1, p2 : electrical); end entity capacitor; architecture ideal of capacitor is quantity v across i through p1 to p2; begin if domain=quiescent_domain use v == 0.0; --initial condition else i == cap * v'dot; -- Fundamental equation end use; end architecture ideal; </pre>
<p>Modelling of the Power Switch</p> <pre> library IEEE; use IEEE.std_logic_1164.all; use IEEE.electrical_systems.all; -- behavioral model of the power switch entity PowerSwitch is generic (Ron : REAL := 0.05; -- 'on' resistance Goff : REAL := 1.0E-6; -- 'off' conductance Csw : REAL := 200.0E-12); -- 200pF port (terminal aT,bT: electrical; -- switch terminals signal Control: in std_logic); -- switch control signal end entity PowerSwitch; architecture Behaviour of PowerSwitch is quantity Vswitch across Iswitch through aT to bT; -- switch voltage </pre>	<p>Modelling of the Diode</p> <pre> library IEEE; use IEEE.math_real.all; use IEEE.electrical_systems.all; -- FUNDAMENTAL_CONSTANTS package needed for Boltzmann constant -- (PHYS_K = Joules/Kelvin) and electron charge (PHYS_Q = coulomb) use IEEE.FUNDAMENTAL_CONSTANTS.all; entity diode is generic (Isat: current := 1.0e-14); -- Saturation current [Amps] port (terminal p, n : electrical); end entity diode; architecture ideal of diode is -- Declare internal quantities and constants </pre>

<pre> begin if domain=quiescent_domain use -- initial condition Vswitch == 0.0; elsif Control = '1' use -- use low-time-constant equation if switch is on Ron*Csw*Vswitch'dot + Vswitch == Ron*Iswitch; -- low time constant else -- off Csw*Vswitch'dot + Vswitch*Goff == Iswitch; -- high time constant end use; end architecture Behaviour; -- entity PowerSwitch </pre>	<pre> quantity v across i through p to n; constant TempC : real := 27.0; -- Ambient Temperature [Degrees] constant TempK : real := 273.0 + TempC; -- Tempereare [Kelvin] constant vt : real := PHYS_K*TempK/PHYS_Q; -- Thermal Voltage -- This function is to limit the exponential function to avoid convergence -- problems due to numerical overflow. At x=100, it becomes a straight line -- with slope matching that at the intercept. function limit_exp(x : real) return real is variable abs_x : real := abs(x); variable result : real; begin if abs_x < 100.0 then result := exp(abs_x); else result := exp(100.0) * (abs_x - 99.0); end if; -- If exponent is negative, set exp(-x) = 1/exp(x) if x < 0.0 then result := 1.0 / result; end if; return result; end function limit_exp; begin -- ideal architecture -- Fundamental equation i == Isat*(limit_exp(v/vt) - 1.0); end architecture ideal; </pre>
---	---

Above we have shown modelling of various components used the the circuit diagram of the SMPS model. After simulation in Hamster software we get the desired result which is shown below :-

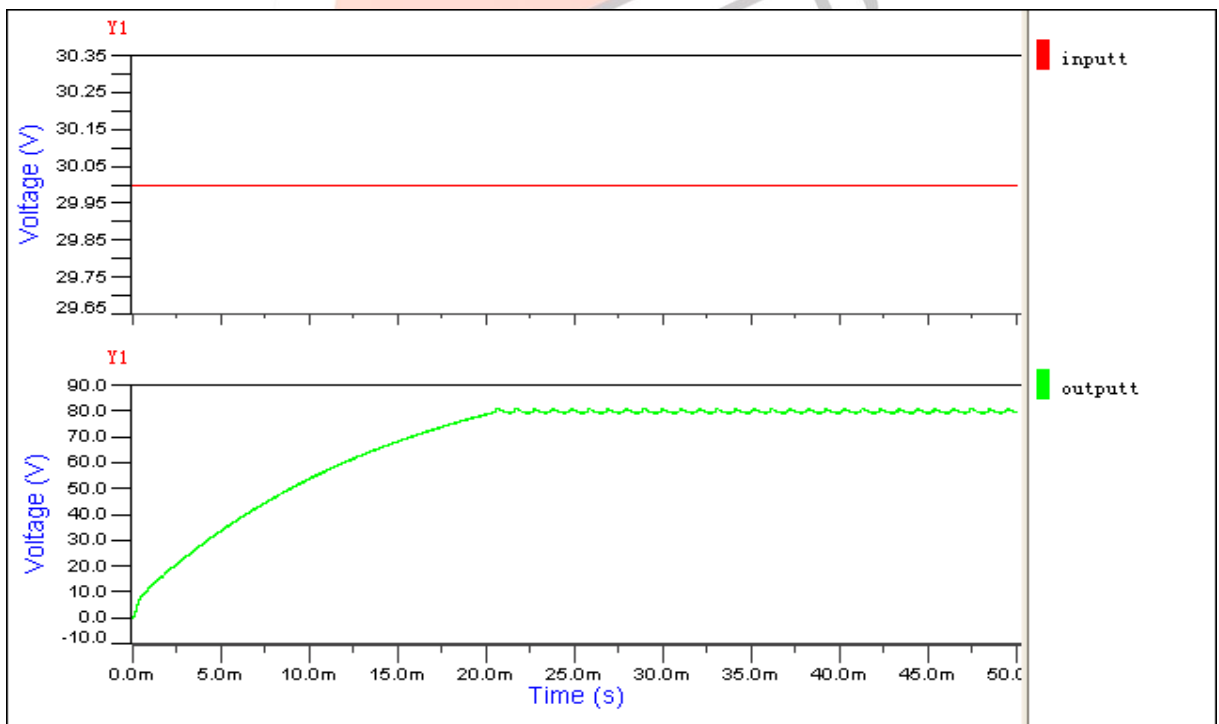


Fig. 5 Simulation Result in Hamster software.

IV. CONCLUSION

We have given an overview of VHDL-AMS, a hardware description language for analog, digital, and mixed-signal applications. We have focused on the main aspects of the language and illustrated the introduction of the language concepts by example of the SMPS and giving the modelling codes in VHDL AMS language for some of the components used in SMPS. VHDL-AMS includes much more, and the interested reader is encouraged to explore the language by studying the language reference manual [4] and other available literature.

V. ACKNOWLEDGMENT

The authors of this paper take this opportunity to thank all the concerned who helped us in our research. We would like to acknowledge our Institute, Department of Electronics and Telecommunication Engineering for their constant motivation and support and helping us all to frame the issues and giving us proper guidance.

At last, we also thank all our colleagues who assisted and backed us during our research.

REFERENCES

- [1] VHDL Language Reference Manual, IEEE Standard 1076-1993.
- [2] Standard Description Language Based on the Verilog(TM) Hardware Description Language, IEEE Standard 1364-1995.
- [3] J. C. Strauss et al., "The SCI continuous system simulation language (CSSL)," Simulation, pp. 281–303, Dec. 1967.
- [4] Definition of Analog and Mixed Signal Extensions to IEEE Standard VHDL, IEEE Standard 1076.1-1999.
- [5] 1076.1 Design Objective Document V 2.3 (1995). [Online]. Available HTTP: <http://vhdl.org/vi/analog>
- [6] 1076.1 Design Objective Rationale V 1.2 (1995). [Online]. Available HTTP: <http://vhdl.org/vi/analog>
- [7] K. E. Brenan, S. L. Campbell, and L. R. Petzold, Numerical Solution of Initial-Value Problems in Differential-Algebraic Equations. Philadelphia, PA: SIAM, 1996.

