

12 Bit Prefetch DDR3 & Speed Enhancement in DDR3 SDRAM using FIFO Synchronization Technique

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Abstract - The demand for high speed and small size memories has been increasing by the day. All device size is decreasing day-by-day in electronics industry for the best handling and carrying. Hence, these memory devices are rapidly developing to give high density and high memory bandwidths. However, with the increase in technology, complexity of instructions to control the memory devices also increases. This paper presents the technique and architecture of the DDR3 Controller which can be used to enhance the speed and discuss advantages of DDR3.

Index Terms - Double Data Rate(DDR), First-In First-Out (FIFO), Field Programmable Gate Array(FPGA), Finite State Machine(FSM), Input-Output(I/O), Integrated Software Environment(ISE), Static Dynamic Random Access Memory(SDRAM), Look-Up-Table(LUT), Random Access Memory(RAM).

I. INTRODUCTION

The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. In computing systems, DDR3 SDRAM or double data rate three synchronous dynamic random access memory is a technology used for high bandwidth storage of the working data of a computer or other digital electronic devices. DDR3 is part of the SDRAM family of technologies and is one of the many DRAM (dynamic random access memory) implementations.

The primary benefit of DDR3 is the ability to transfer I/O data at eight times the data rate of the memory cells it contains, thus enabling higher bus rates and higher peak rates than earlier memory technologies. However, there is no corresponding reduction in latency, which is therefore proportionally higher. In addition, the DDR3 standard allows for chip capacities of 512 megabits to 8 gigabits, effectively enabling a maximum memory module size of 16 gigabytes. However, going with the present trend of increasing memory requirements, we need RAM which is faster, better and has more capacity. In view of this, we have decided to design DDR4 SDRAM controller. The associated interface techniques used by DDR3 SDRAM is not directly compatible with any earlier type of random access memory (RAM) due to different signalling voltages, timings, and other factors. With two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed in megabytes per second (MB/s). In addition, the DDR3 standard permits chip capacities of up to 8 gigabits. The primary benefit of DDR3 SDRAM over its immediate predecessor, DDR2 SDRAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth or peak data rates.

II. THEORY

The frequencies of DDR3 memory could be raised beyond those of DDR2 due to doubling of the data prefetch that was moved from the info storage device to the input/output buffer. While DDR2 SDRAM uses 4-bit samples, DDR3 SDRAM uses 8-bit prefetch also known as 8n-prefetch. In other words, DDR3 SDRAM technology implies doubling of the internal bus width between the actual DRAM core and the input/output buffer. As a result, the increase in the efficient data transfer rate provided by DDR3 SDRAM doesn't require faster operation of the memory core. Only external buffers start working faster. As for the core frequency of the memory chips, it appears 8 times lower than that of the external memory bus and DDR3 buffers (this frequency was 4 times lower than that of the external bus by DDR2) So, DDR3 memory can almost immediately hit higher actual frequencies than DDR2. SDRAM, without any modifications or improvements of the semiconductor manufacturing processes. However, the above described technique also has another side to it: unfortunately, it increases not only memory bandwidth, but also memory latencies. As a result, we shouldn't always expect DDR3 SDRAM to work faster than DDR2 SDRAM, even if it operates at higher frequencies than DDR2.

III. METHOD

A low power and high speed DDR3 SDRAM controller taking every opportunity to decrease system latencies while maintain low power in the duration of peak read/write times. This was achieve throughout extremely dedicated hardware space explorations which enabled to optimize the speed of the controlling FSM to a large extent.

Top Module

The top module of DDR3 SDRAM Controller is show in Fig 1. It consists 3 modules, first the main controller module, second the signal module and third is the data path module. The user sends the data to be written on or read from the DDR3 SDRAM with the memory location (address). The controller module has two state machines with a refresh counter. The address and command signals required for DDR3 are generated by signal generation module and The data path module perform data latching and dispatching of the data between the DDR3 and processor.

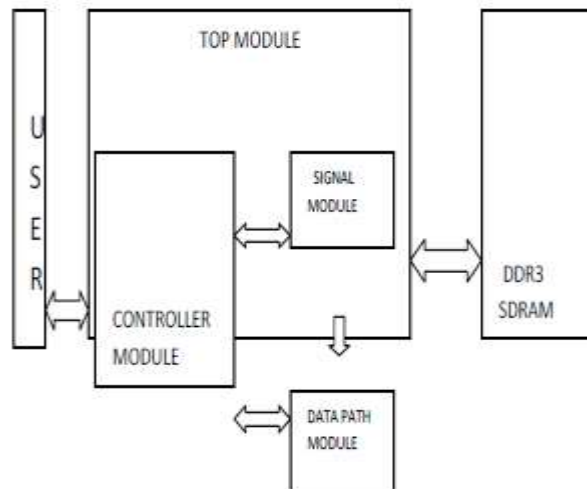


fig.1: Block Diagram of Top Module

DDR3 Features Comparison

DDR3 is the next-generation, high performance solution for CPU system. it push the cover in key areas like power consumption, bandwidth and signalling speeds bring new levels of performance to notebook, desktop, and server computing. DDR3 offer a significant performance enhancement over the earlier DDR2 and DDR memory systems. One of the main DDR3 feature including enhanced signal integrity so as to have high performance not including an unnecessary burden on the system designer. Table.1 compares some difference among DDR3 and the previous two hierarchies.

Table 1 Comparison of Different DDR Features

Features	DDR1	DDR2	DDR3
Data Rate	200-400 Mbps	400-800 Mbps	800-1600 Mbps
Burst Length	BL=2,4,8	BL=4,8	BL=4,8
No Of Banks	4banks	512MB:4Banks 1GB:8Banks	512MB/1GB:8 banks
Prefetch	2Bit	4Bit	8Bit
Vdd/Vddq	2.5+/- 0.2V	1.8+/-0.1V	1.5+/-0.075V

DDR3 SDRAM

DDR3 provides two burst modes for each reading and writing: burst chop (BC4) and burst length eight (BL8). BC4 allows bursts of four by treating information as if half it's masked. This creates smooth transitioning if shift from DDR2 to DDR3 memory. However, burst mode BL8 is the primary burst mode. BL8 allows the most information to be transferred within the smallest amount of time; it transfers the best range of 64-bit information packets (eight) to or from consecutive addresses in memory, which means that addressing happens once for each eight information packets sent. In order to support a burst length of eight data packets, DDR3 SDRAM has an 8-bit prefetch buffer.

The frequencies of DDR3 memory could be raised on the far side those of DDR2 as a result of doubling of the information prefetch that was enraptured from the information memory device to the input/output buffer. While DDR2 SDRAM uses 4-bit samples, DDR3 SDRAM uses 8-bit prefetch also best-known as 8n-prefetch. In other words, DDR3 SDRAM technology implies doubling of the internal bus width between the particular DRAM core and therefore the input/output buffer. The main controller module has two state machines and a refresh counter. The signal generation module generates the address and command signals required for DDR3.

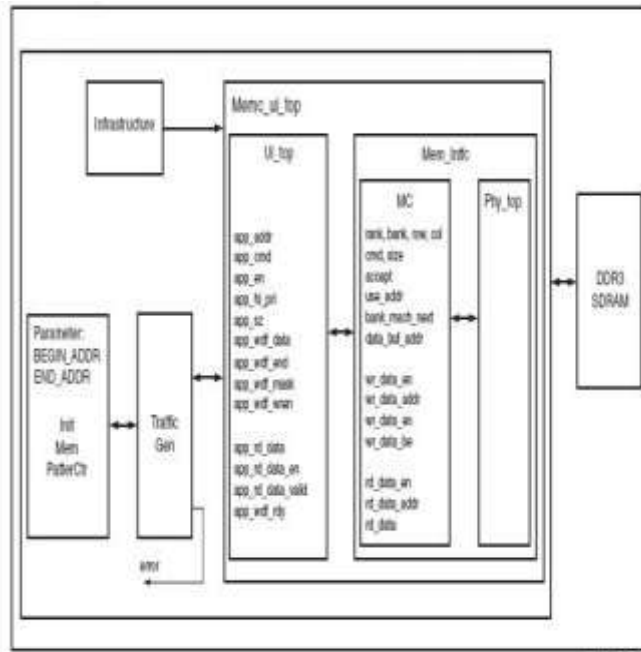


fig.2: Block diagram of proposed design

IV. SIMULATION RESULT

In this work we designed a high speed DDR3 SDRAM. The code is written in VERILOG language. The tool which used to synthesize it and verify is Xilinx. The entire task file include all operations was set up. after that, all mode registers were initialized. in conclusion, test bench with several test cases were set to verify the estimated results. The Fig shows the RTL graphic of the top module and the controller respectively.

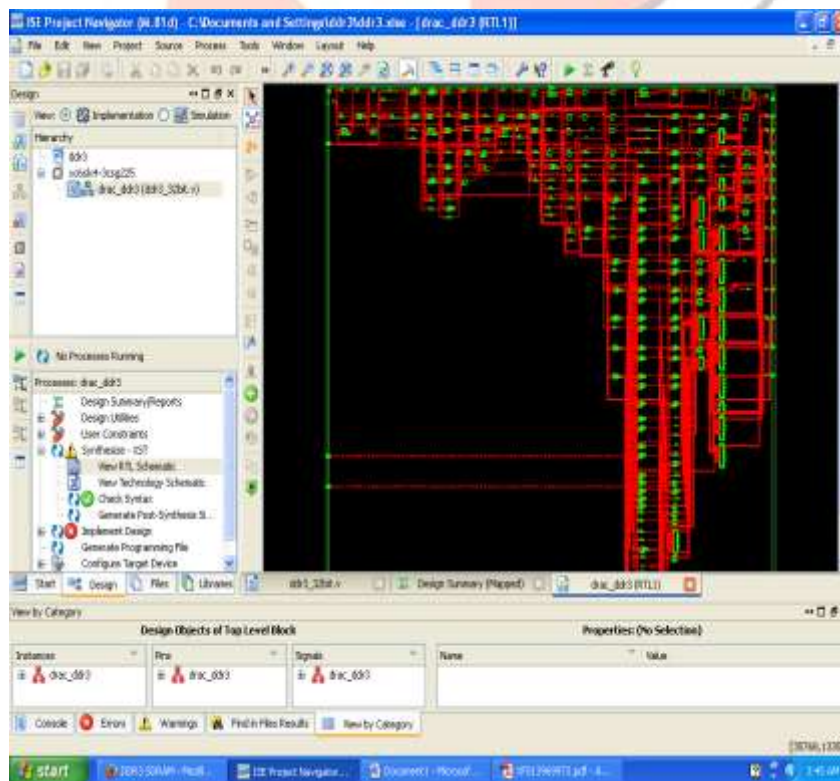


fig.4: Technology view of the SDRAM controller

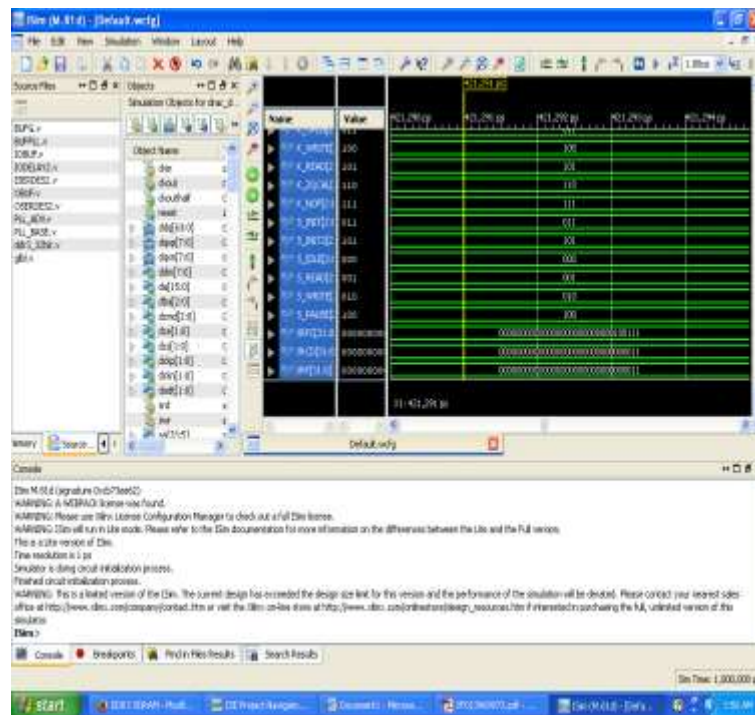


fig.5: Simulation of the SDRAM controller

V. CONCLUSION

This document projected high speed area resourceful DDR3 SDRAM, the structural design is evaluating in FPGA using Xilinx ISE mean group. In manipulative, the system using 14% of segment registers and 15% of slices LUTs. Thus, it occupies fewer regions and intense less power. These projected structures provide high speed procedure as of synchronization FSM with FIFO.

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